FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office	ATTY. DOCKET NO.	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	500.28166CX2	Not yet assigned
	APPLICANT: HOTTA, et al	
	FILING DATE: May 14, 2001	GROUP: 2152

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		4722050	1/88	Lee et al	395	375	
		4620275	10/86	Wallach et al	395	800	
		3614745	10/71	Podia et al	395	650	
		4928226	5/90	Kamada et al	364	200	
		3771138	11/73	Celtruda et al			
		4677545	6/87	Blahut			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT YES	ABSTRACT NO
		0149049	7/85	EPO				
		0260409	3/88	EPO				
		8809035	11/88	WIPO				
		0082903	7/83	EPO				
		63733233	2/88	Japan				XX

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		Technical Summary, Multi-flow Computer, Inc., 4/30/87, pp/ 1-(3-7).
		O. Serlin, "The Serlin Report on Parallel Processing", ITOM International Co., Issue No. 7, 12/87, pp. 10-18.
		IEEE Journal of Solid-State Circuits, "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with on-chip Cache", Horowitz, et al, vol. sc-22, No. 5, October 1987, New York.
		J. Bond, "Parallel Processing Concepts Finally come together in Real Systems", Computer Design, June 1, 1987, pp. 51-74.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		5,101,341	3/92	Circello et al	395	375	
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		5,072,364	12/91	Jardine et al	395	375	5-24-89
		4,873,629	10/89	Harris et al			
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		0,459,232	12/91	EPO				
		3,288,246	12/91	Japan				XX
		0,455,599	11/91	EPO				
	6	3,131,230	6/88	Japan				

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	R. Acosta, et al, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors", IEEE Transactions on Computers vol. C-35, No. 9, Sept. 1986, pp. 815-828.
	D. Ditzel, et al "The Hardware Architecture of the Crisp Microprocessor" ACM, 0084-7495, pp. 309-319.
	Capozzi et al, "Non-sequential High-performance Processing", IBM Technical Disclosure Bulletin, vol. 27, No. 5, 10/84, pp. 2842-2844.

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500.28166CX2	Not y t assigned
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FILING DATE: May 14, 2001	GROUP: 2152

J1011 U.S. PTO 09/853769 05/14/01

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
h		4 9 4 2 5 2 5	7/90	Shintani et al	395	Dig. 1	11/20/87
h		5 2 8 7 4 6 5	2/94	Kurosawa et al			
h		5 4 0 4 4 7 2	4/95	Kurosawa et al			
h		5 5 6 1 7 7 5	10/96	Kurosawa et al			
h		4 4 7 6 5 2 5	10/84	Ishii	364	Dig. 1	
h		4 5 9 4 6 5 5	6/86	Hdo et al	364	DIG. 1	
h		4 6 2 6 9 8 9	12/86	Rorii	395	375	
h		4 6 4 4 4 6 6	2/87	Saito	395	725	
h		4 7 9 4 5 1 7	12/88	Jones et al	395	725	
h		4 9 1 6 6 0 6	4/90	Yamaoka et al	395	375	
h		4 9 2 8 2 2 3	5/90	Dao et al	395	375	

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT YES	ABSTRACT NO
h		0 1 4 7 8 5 8	7/85	EPO				
h		0 0 4 2 4 4 2	12/81	EPO				
h		0 2 3 9 0 8 1	9/87	EPO				
h		0 1 0 1 5 9 6	8/83	EPO				

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h		J. David, "Reducing the Branch Penalty in Pipelined Processors", Computer (July1988), pp. 47-55.
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h		G. Tjoden et al, "Detection and Parallel Execution of Independent Instructions", IEEE Transaction, vol. C-19, N . 10, Oct ber 1970, pp. 889-895.

EXAMINER: [signature] DATE CONSIDERED: 8/26/06

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